

PRODUCT SPOTLIGHT

Cellular Memory Swaps In The Next Generation

Partners Have Spawned High-Performance, Drop-In-Replacement Memory Chips For 2.5G And 3G Network Applications.

ALTHOUGH they have been hyped for many years, high-data-rate cellular networks are now becoming a reality. As more communities are upgraded with 2.5G and 3G infrastructure systems, consumer interest is growing in the networks' potential benefits. But the infrastructure side is only half of the equation. For next-generation cellular networks to succeed, 2.5G and 3G handsets must offer high-performance features, such as high-resolution color displays and fast processors. These features will promote high-speed gaming and Internet browsing. Of course, their supporting memory chips must be of equally high performance. At the same time, these improved memory chips must not increase the size of existing chips' form factors or consume too much additional power.

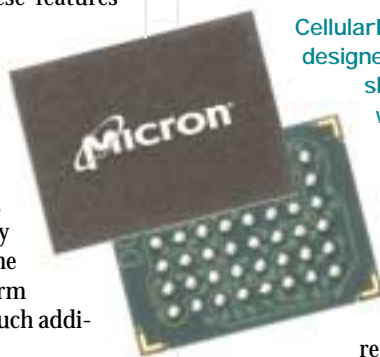
To satisfy these challenging design requirements, the CellularRAM family of pseudo-static random-access-memory (PSRAM) products has emerged. All of these devices are backwards compatible with six-transistor (6T) and early-generation asynchronous or page PSRAMs. At the same time, the CellularRAM family offers many new features like burst READ modes. Such features should provide an evolutionary path to pseudo-SRAMs.

The CellularRAM devices were designed as a DRAM technology with an SRAM interface. They provide the densities and performance levels that are mandated by next-generation cell phones. Compared to current SRAM products,

they even boast a lower price per bit.

The devices were developed by a trio of companies: Cypress Semiconductor, Infineon, and Micron Technology. All three members participated in creating the CellularRAM specification. Their goal was to provide pin-and-function-compatible products from multiple source vendors.

The CellularRAM specification describes the necessary operational characteristics for these next generation memory devices, including VDD, pack-



CellularRAM chips are designed to be pin- and shape-compatible with today's cellular-memory devices.

age and pinout, refresh, page mode, mode-register (bus and refresh), I/O, and truth tables. Under the terms of the development agreement, each vendor will manufacture CellularRAM devices that meet these specifications but utilize their own designs and process technologies and product-development timetables.

To mark the companies' first success, a 32-Mb CellularRAM device family was recently announced for wireless handsets (SEE FIGURE). This multi-generation family of low-power, PSRAM is based on a single-transistor (1T) DRAM cell. In contrast, most current handsets use a 6T SRAM cell. The 1T architecture allows handset makers to add more features to their phones without degrading system

speed or increasing the product's size.

The devices were designed to be pin compatible with SRAM devices. In fact, CellularRAMs are heralded as drop-in replacements for the asynchronous SRAM that is used in existing cell phones. CellularRAM devices also vow to have the same voltage range, package, and ball assignments. This should enable handset designers to transition from SRAM to CellularRAM devices without suffering many development headaches.

The new architecture benefits from the reduced size and density of DRAM cell technology. Current 6T pseudo-SRAM devices require six transistors. But they provide a relatively low-density, high-die-size cell. CellularRAM cells, on the other hand, require one transistor and one capacitor. This approach results in a high-density and low-die-size device.

The minimal component design also packs a powerful performance punch. The 32-Mb CellularRAM samples that are currently available operate at up to 104-MHz clock rates with a low initial latency of 70 ns. These devices can achieve up to 208 Mbps (1.5 Gbps) of peak bandwidth. In addition, they employ a burst read-and-write mode. This mode emulates today's best Flash-memory interfaces, including Intel's W18 and Micron's Flash Burst-compatible protocols.

The 32-Mb devices are organized in a 2-Mb \times 16 configuration. The 16-Mb and 64-Mb density components are organized as 1 Mb \times 16 and 4 Mb \times 16. Micron and Infineon are currently sampling devices. Cypress plans to have samples available in the first half of 2004.

The next generation of the CellularRAM product family—the 128-Mb device—is currently under co-development by the three companies. It should sample in the second quarter of 2004. ■

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